Dr. Dimoulas obtained his Ph.D in Applied Physics from the University of Crete and the Foundation for Research & Technology-Hellas in Greece in 1991 on MBE heteroepitaxial growth and characterization of GaAs and related compounds on Si. He was Human Capital & Mobility Fellow of the EU at the University of Groningen in Holland until 1994, a Research Fellow at the California Institute of Technology (CALTECH), Chemical Engineering, Pasadena USA until 1996 and Research Associate at the University of Maryland at College Park (UMCP) USA, until February 1999. In addition, Dr. Dimoulas was visiting research scientist at NRL, Washington DC, in 1992 and at IBM Zurich Resarch Laboratory, Switzerland, in 2006 and 2007, on sabbatical leave from NCSR DEMOKRITOS. Since 1999, Dr. Dimoulas is research director and head of the MBE and Surface Analysis laboratory at the Institute of Materials Science of the National Center for Scientific Research DEMOKRITOS, Athens, Greece. He has authored or co-authored more than 110 technical publications in refereed journals and 3 monographs in Springer book chapters on high-k gates on Si, Ge and GaAs. He has given more than 30 invited presentations in international conferences, Summer Schools and Tutorials. He is co-editor in a Springer book “Advanced gate stacks for high mobility semiconductors” and guest editor in two special volumes of international journals. He has co-authored by invitation a review article on “Contacts to source and drain for Ge and III-V MOSFETs” for the special issue of the MRS bulletin scheduled for publication in the July 2009 issue, featuring alternative high mobility channel materials and devices.He has been the main organizer of E-MRS 2003 symposium on “Functional Oxides on Semiconductors” and of the MRS 2005 symposium on “Advanced Gate Stacks for High Mobility Semiconductors”. Also, he was the general chair of the international INFOS 2007 conference held in Athens in 2007. He is member of the international advisory (steering) committees of ICSI, INFOS, and ESSDERC-ESSCIRC conferences and member of the technical program committees of INFOS 2005, ESSDERC 2008, 2009, 2010, 2011, and IEDM 2010, 2011 and 2012). He has served as chair of the technical program committee of the European ESSDERC 2009 conference in Athens, chair of the Advanced CMOS subcommittee of ESSDERC 2011 at Helsinki and Chair of the Process Technology Subcommittee of IEDM 2012. His expertise includes MBE growth of semiconductor (including III-Vs) and dielectric materials, nanodevice processing by photo-and e-beam lithography and materials characterization & device electrical testing. He has been involved for about ten yearsin the development of high-k gate stacks for Si, Ge and III-V MOS technologyleading several European-funded STREP projects (INVEST, ET4US, DUALLOGIC) in the area of advanced CMOS. His current interests focus on Post CMOS materials and devices for technologies beyond 2020. The research is financially supported by EU FET project 2DNANOLATTICES (http://www.2dnanolattices.eu ), GSRT-ARISTEIA National project TOP-ELECTRONICS and the prestigious ERC (IDEAS) Advanced Grant SMARTGATE (*Smart Gates for the ‘Green’ Transistor*) focusing on steep slope switches for ultra-low power, energy efficient nanoelectronics (http://www.smartgate-erc.eu )